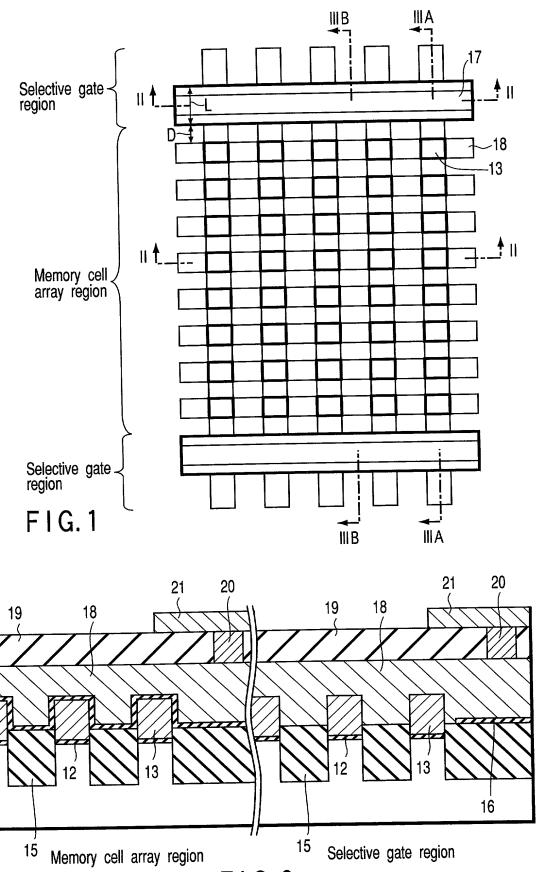
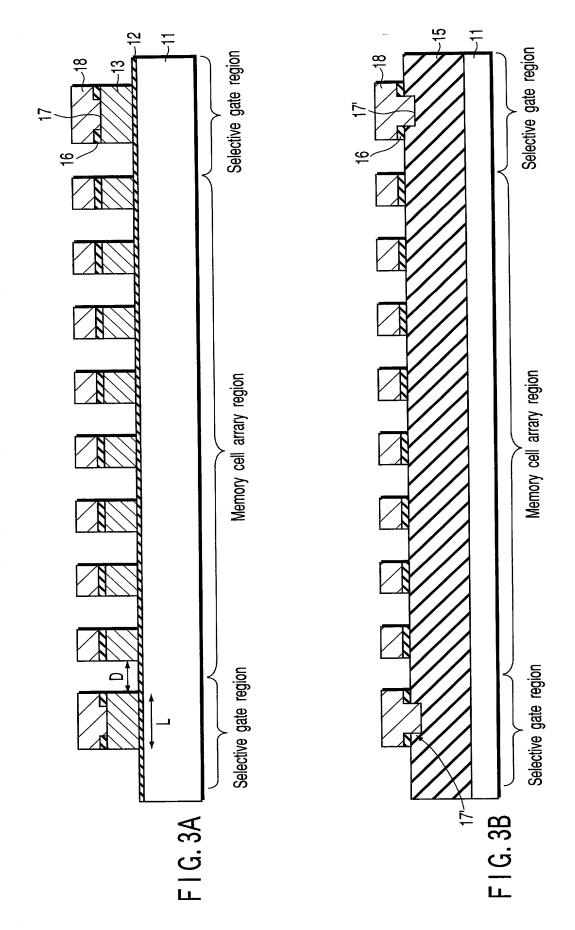
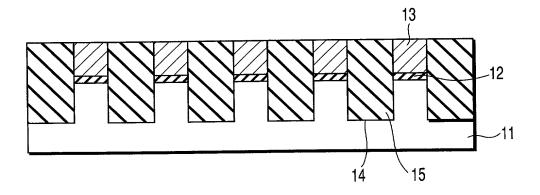
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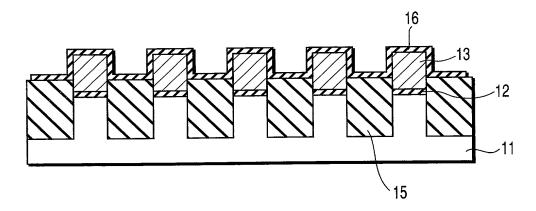


F I G. 2

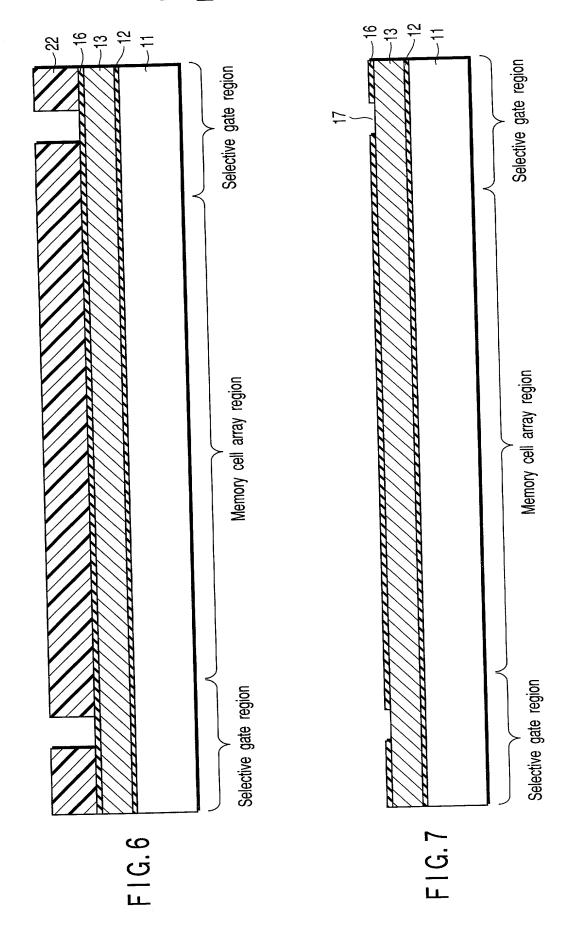


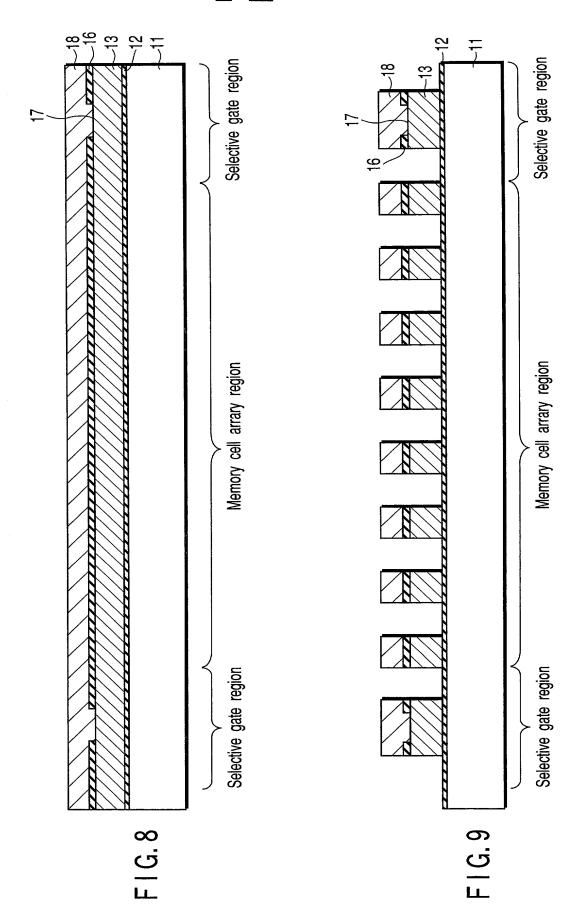


F I G. 4



F I G. 5





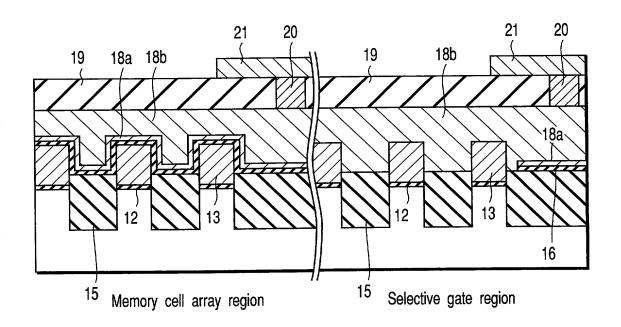
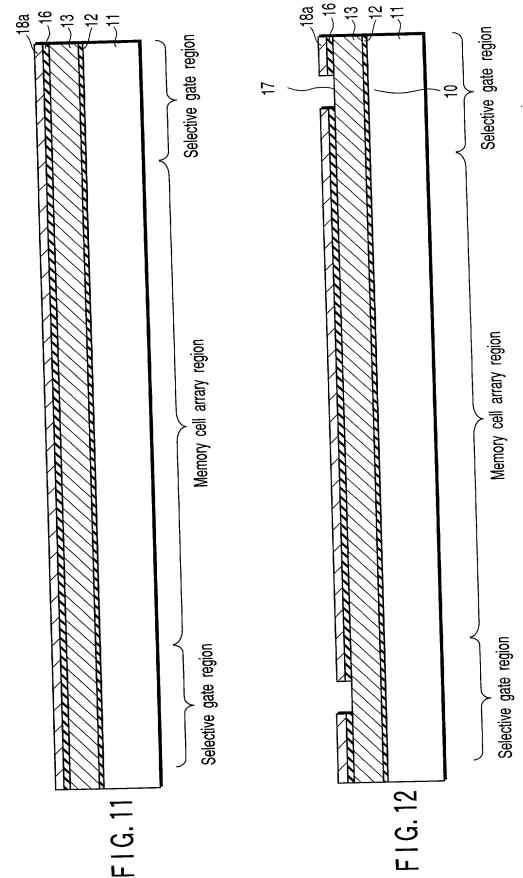
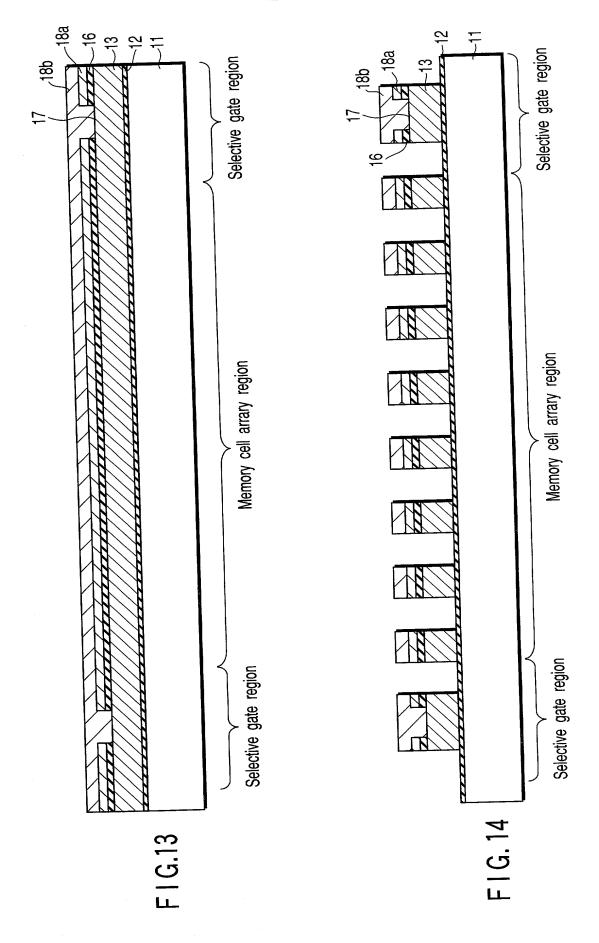


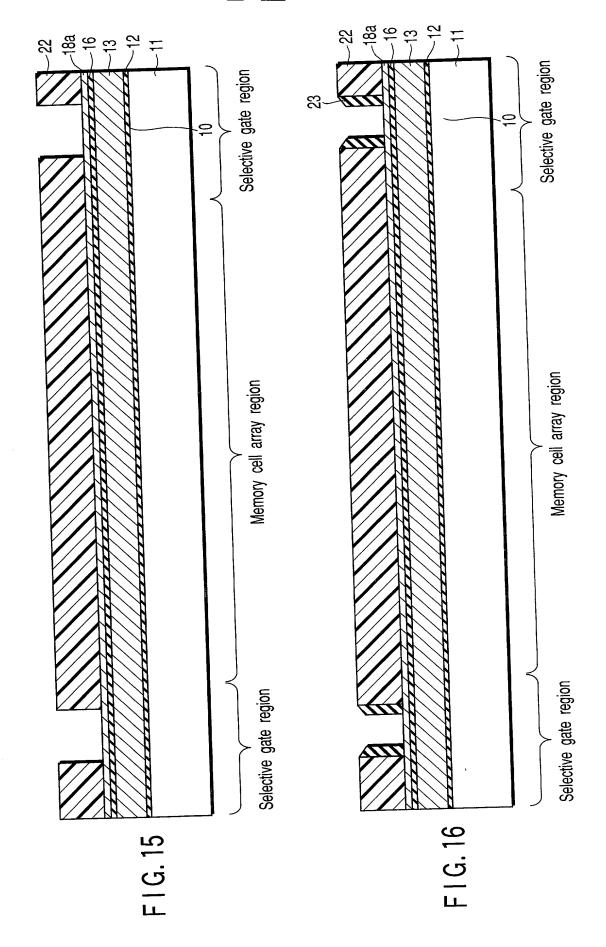
FIG. 10



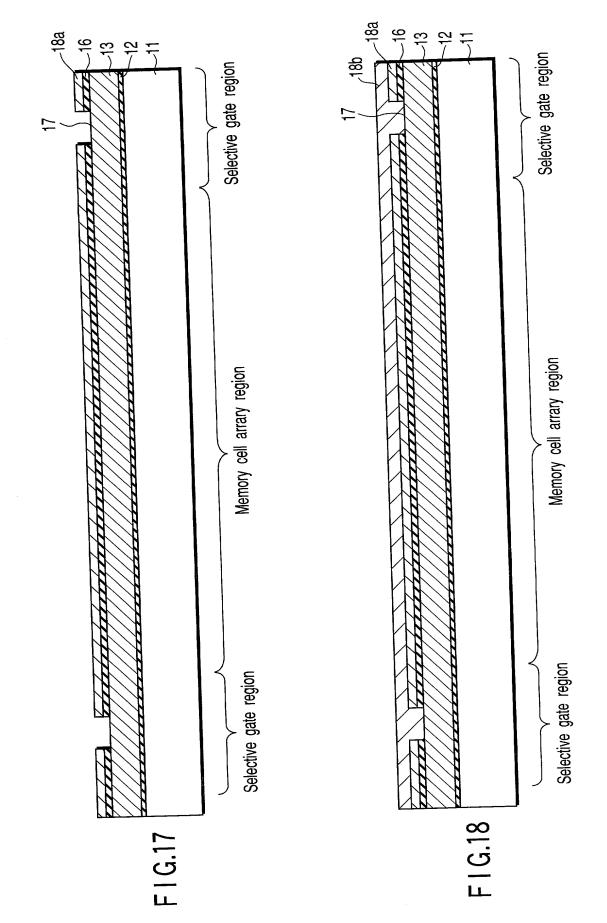
The first who was the first whe

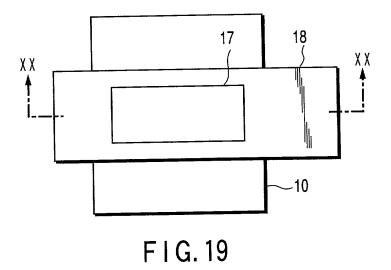


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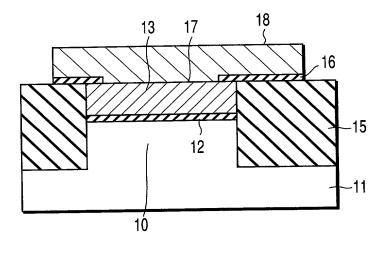
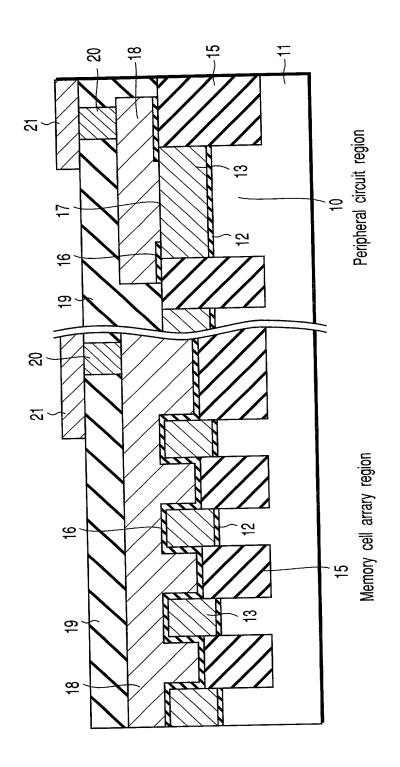
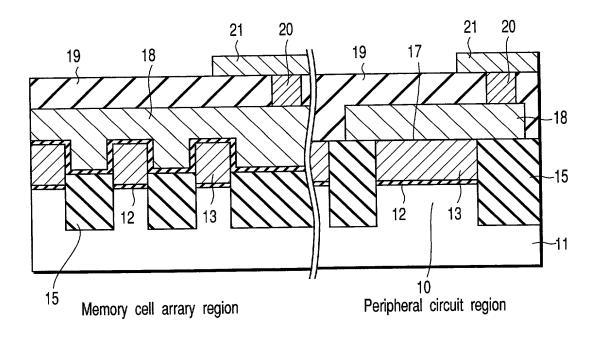


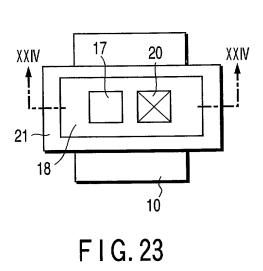
FIG. 20



F1G.2



F I G. 22



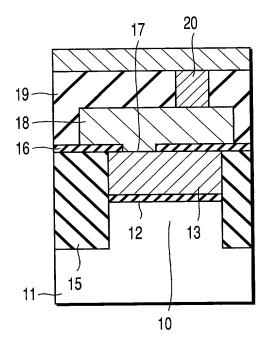
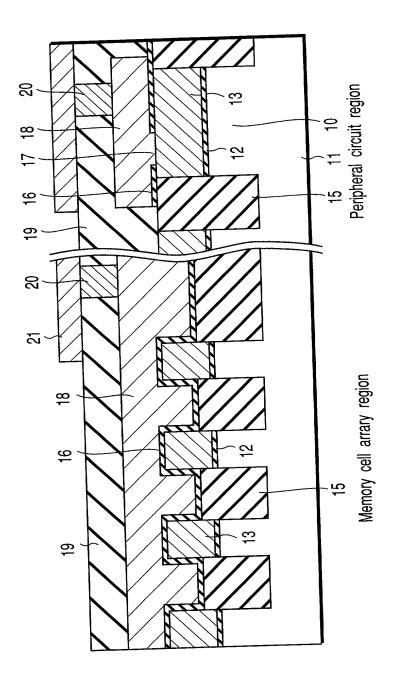
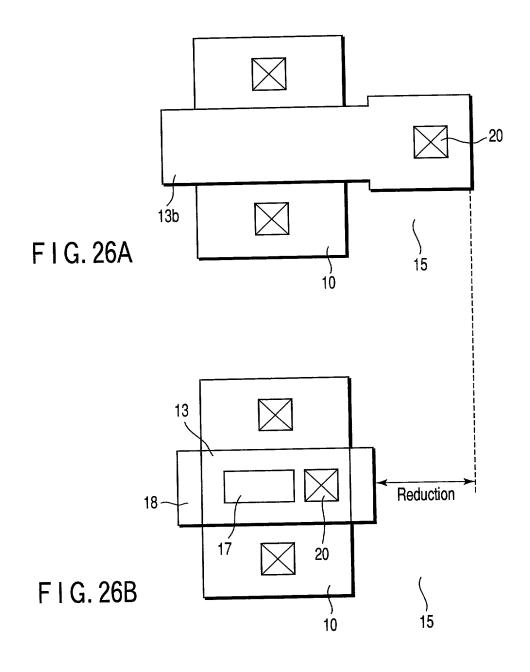


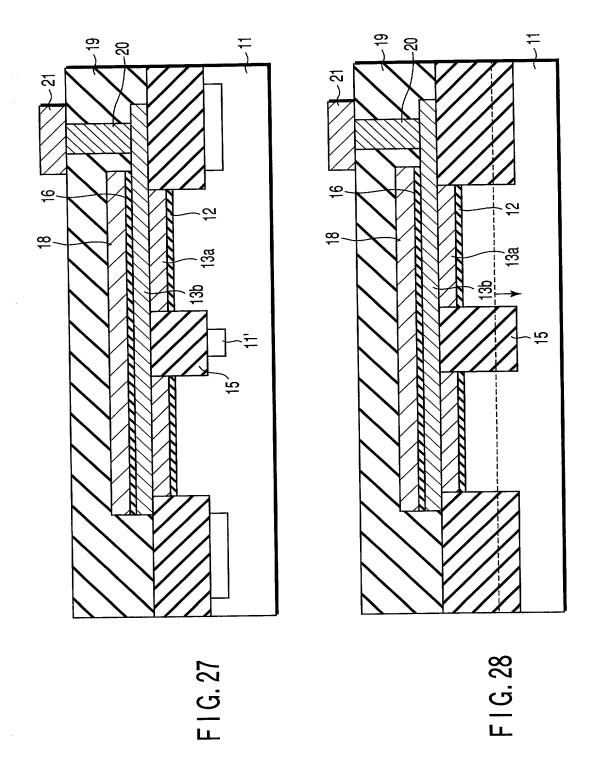
FIG. 24

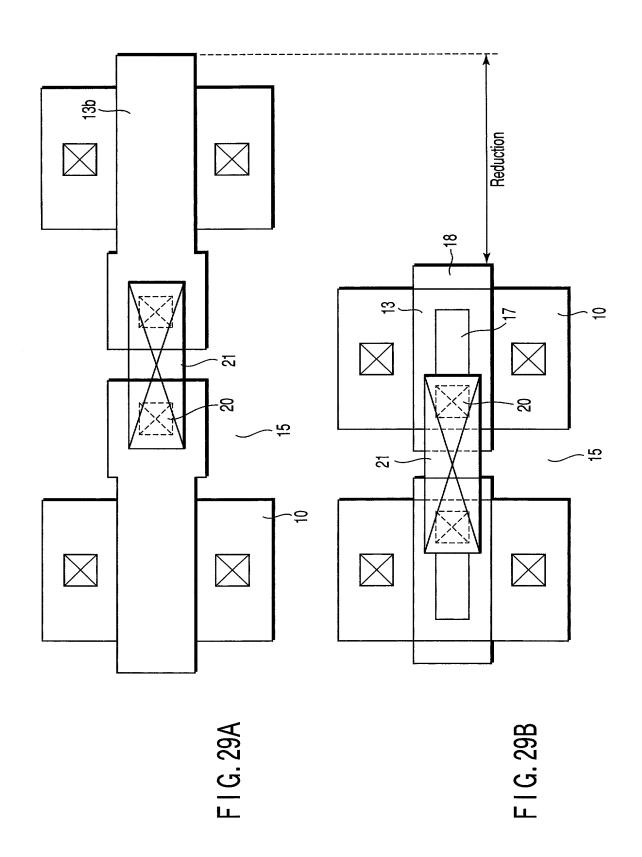
OBLON, SPIVAK, ET AL DOCKET #: 214258US2S INV: Michiharu MATSUI, et al. SHEET 14 OF 33



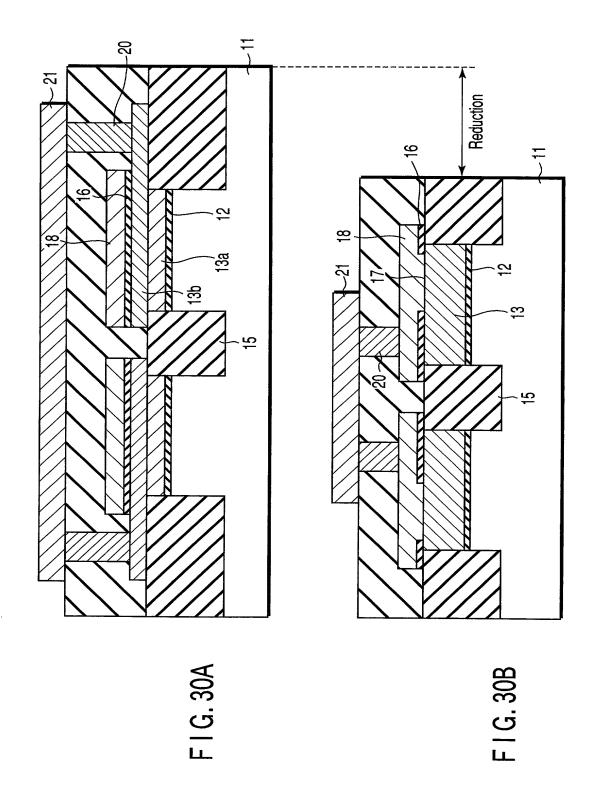
F1G. 25

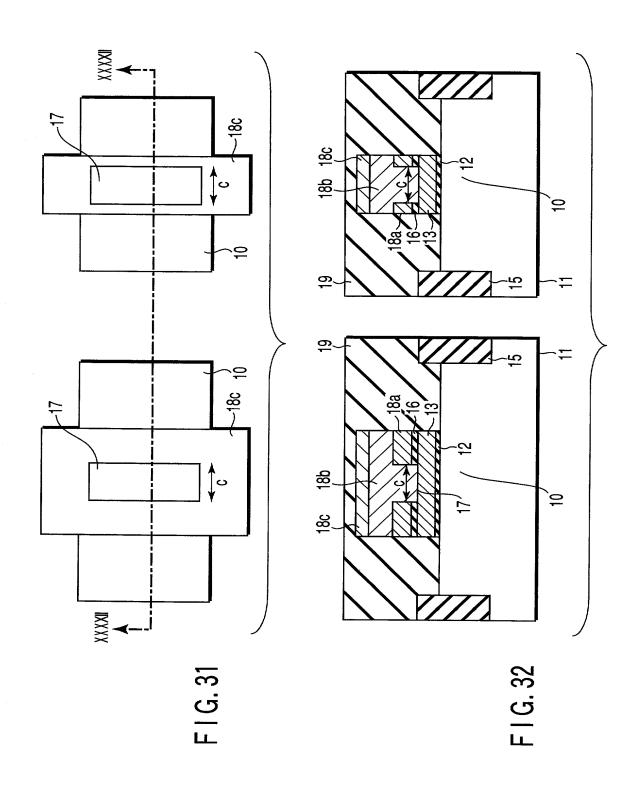


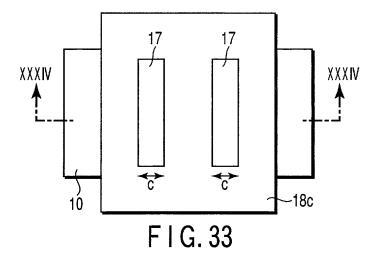


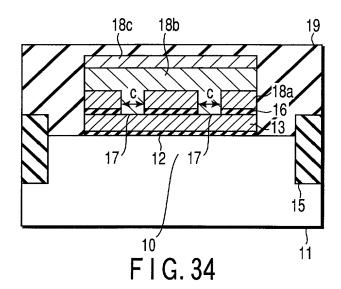


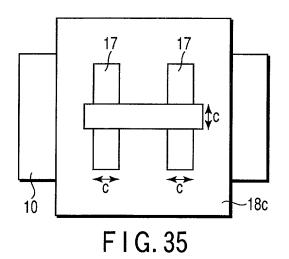
OBLON, SPIVAK, ET AL DOCKET #: 214258US2S INV: Michiharu MATSUI, et al. SHEET 18 OF 33



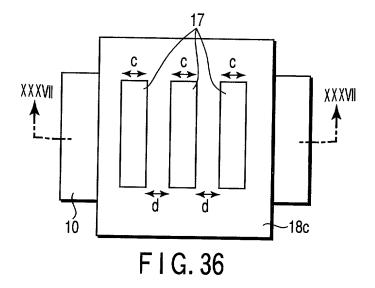


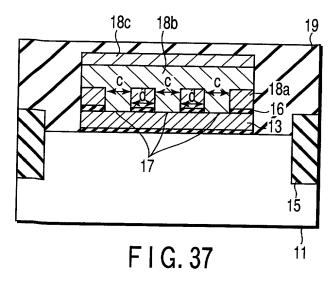


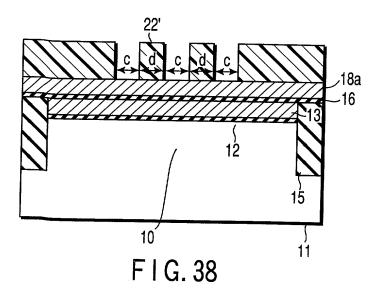


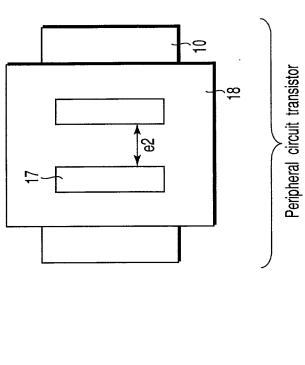


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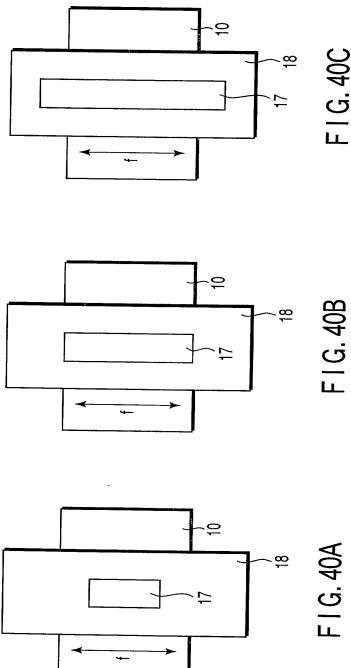


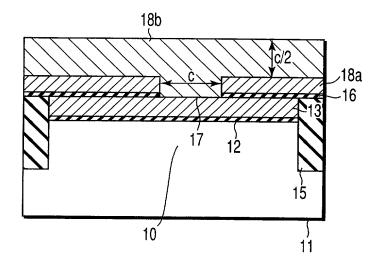


Selective transistor Memory transistor

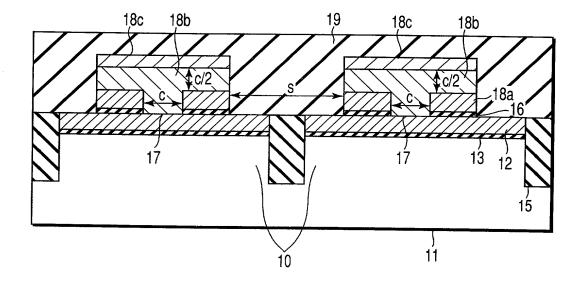
F I G. 39A

FIG. 39B

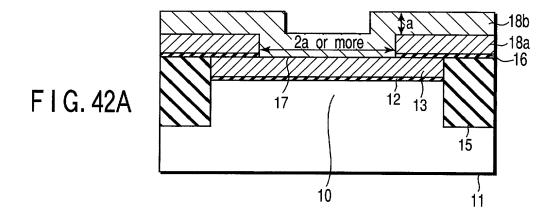




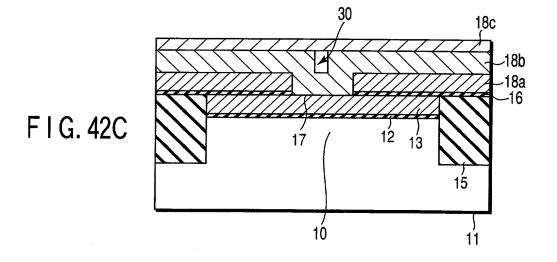
F I G. 41A

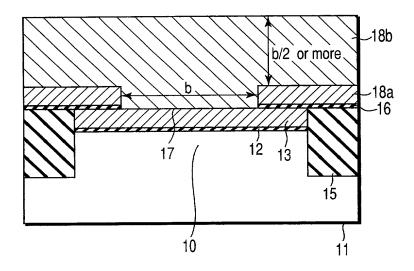


F I G. 41B



F I G. 42B





F I G. 43A

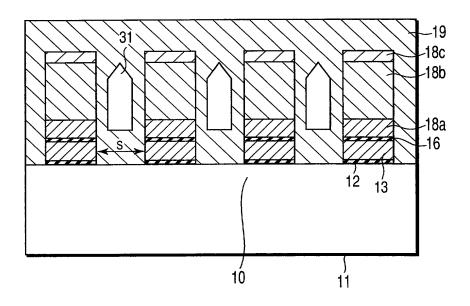
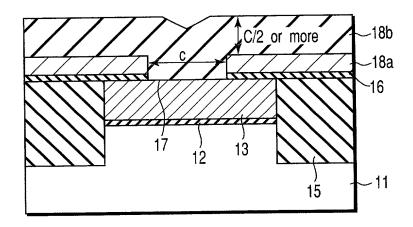
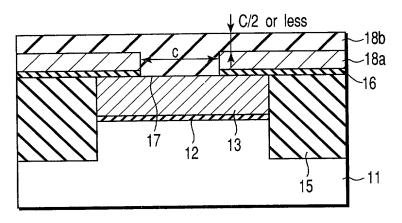


FIG. 43B



F I G. 44A



F I G. 44B

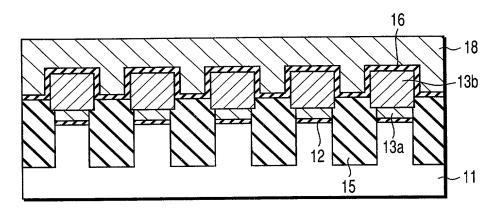
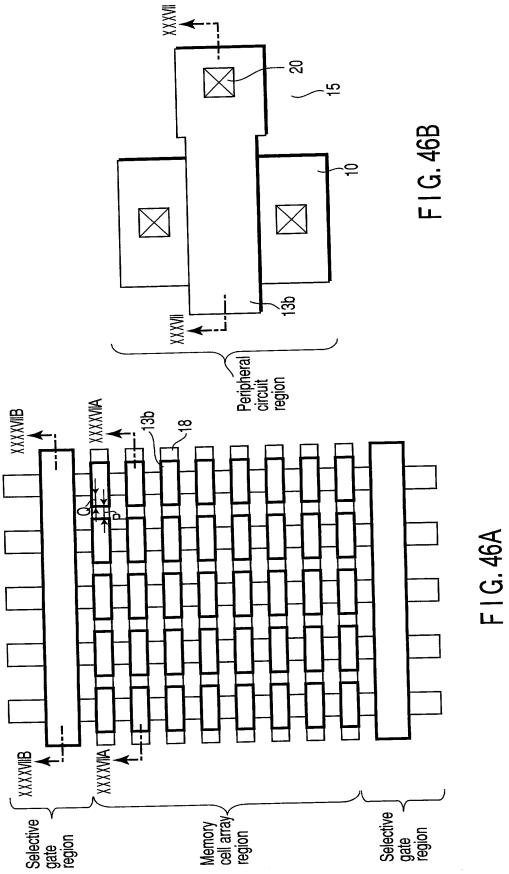
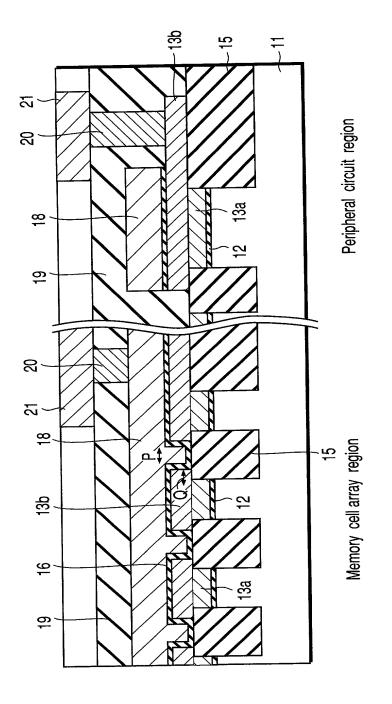


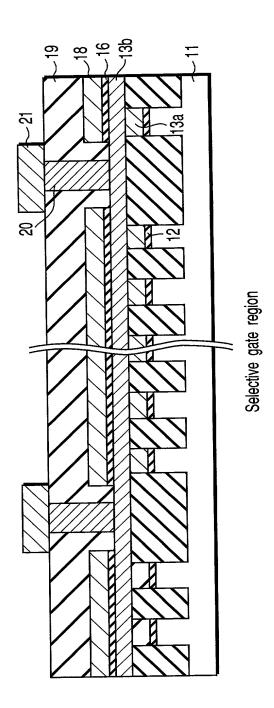
FIG. 45

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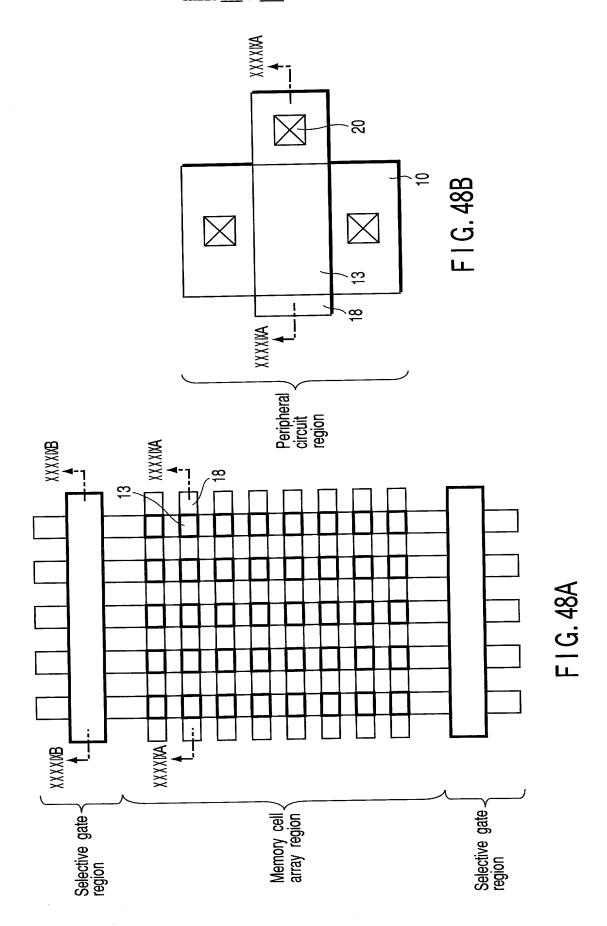


F1G. 47A



F I G. 47E

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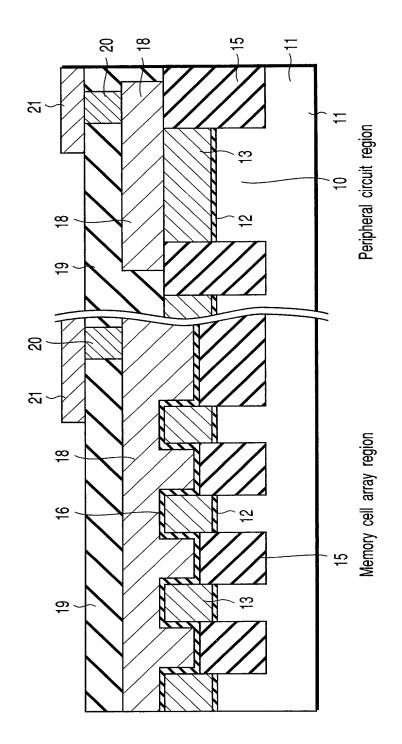
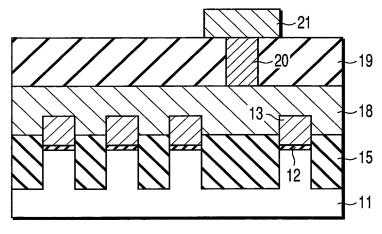


FIG. 49A

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Selective gate region

FIG. 49B

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